FPGA Design Specification

Revision 0.1

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# Revision History

|  |  |  |
| --- | --- | --- |
| Date | Revision | Description |
| 07/22/2021 | 0.1 | Initial version |

# Introduction

This document provides the FPGA design specification for the MIDI Router box.

# Architecture

Figure 1 illustrates the FPGA design architecture. All modules are clocked at 250 KHz.

|  |
| --- |
| SPI  FIFO  MIDI TX Output |
| Figure 1: Architecture of MIDI Router FPGA design |

# Design

## SPI Slave (Write Only)

This module implements an SPI Slave device that supports write-only operations to the FIFO.

## FIFO

This module implements a hardware FIFO using one of the block RAMs of the iCE40 HX device. This is modeled after something like the 74xx222 device, following guidance on <https://www.asic-world.com/>.

## MIDI TX Output

This module instantiates a standard UART transmitter, with glue logic to interface to the FIFO. The output clock is divided (internal to this module) by 8 to provide the required 31.25 KHz baud rate.

|  |
| --- |
| IDLE  READ FIFO  START TX  WAIT TX |
|  |

|  |  |  |  |
| --- | --- | --- | --- |
| Current State | FIFO empty | UART done | Next State |
| IDLE | Y |  | IDLE |
| IDLE | N |  | READ FIFO |
| READ FIFO |  |  | START TX |
| START TX |  |  | WAIT TX |
| WAIT TX |  | N | WAIT TX |
| WAIT TX |  | Y | IDLE |

# Interface

## Electrical

All inputs interface to the FPGA’s 3.3V input ports.

All outputs interface to the FPGA’s 3.3V output ports.

Power up/down requirements are per the iCE40 HX datasheet. No special sequencing requirements exist for this device.

## Software

There is no software interface to the FPGA design.

## Signal List

midi\_in[3:0]: vector of 4 input MIDI signals

spi\_sck: programming/debug interface. Not currently used.

spi\_mosi: programming/debug interface. Not currently used.

spi\_miso: programming/debug interface. Not currently used.

spi\_ss: programming/debug interface. Not currently used.

gpio\_fbin[3:0]: debug interface. Not currently used.

gpio\_bin[15:0]: debug interface. Not currently used.

midi\_out[3:0]: vector of 4 output MIDI signals

# Resource Estimate

## Device Utilization

Flip Flops: 50

LUTs: 75

## Power Estimate

<1mW